Generation of Higher Number of Voltage Levels by Stacking Inverters of Lower Multilevel Structures With Low Voltage Devices for Drives

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***Abstract*—This paper proposes a new method of generating higher number of levels in the voltage waveform by stacking multilevel converters with lower voltage space vector structures. An important feature of this stacked structure is the use of low voltage devices while attaining higher number of levels. This will find extensive applications in electric vehicles since direct battery drive is possible. The voltages of all the capacitors in the structure can be controlled within a switching cycle using the switching state redundancies (pole voltage redundancies). This helps in reducing the capacitor size. Also, the capacitor voltages can be balanced irrespective of modulation index and load power factor. To verify the concept experimentally, a nine-level inverter is developed by stacking two five-level inverters and an induction motor is run using V/f control scheme. Both steady state and transient results are presented.**

***Index Terms*—Cascaded H-bridge inverter (CHB), flying capacitor (FC), induction motor (IM) drive, low voltage devices, multilevel inverter (MLI), pulse width modulation (PWM), topology.**

I. Introduction

In order to obtain a better quality output voltage or current waveform, the switching frequency needs to increase in the conventional two-level and three-level inverters. But in high voltage and high power applications, there is a limitation on switching frequency due to the associated switching losses and power dissipation. Increasing the number of levels in the output voltage reduces harmonic distortion in the output phase voltage waveform [1]. Multilevel converters (MLC) are capable of generating higher levels in the output voltage waveform with low voltage stress on the switches. In addition to better waveform quality and lower total harmonic distortion in the phase voltages, they also have advantages of reduced electromagnetic interference, lower device voltage ratings, and lower switching frequency. Hence, they found widespread applications in motor drives, grid-tied converters, high-voltage dc transmission, reactive power compensation, wind energy conversion, and in many other high power applications [2].

Basic multilevel topologies include diode clamped multilevel inverter (DC-MLI), flying capacitor inverter (FC) and cascaded H-bridge inverter (CHB) [2], [3]. Three-level DC-MLI, commonly known as neutral point clamped inverters (NPC) have become popular in industry. But for higher levels, more clamping diodes are needed and also balancing the capacitors for entire modulation range is an issue [3]. It also suffers from serious drawback of unequal loss distribution among the semiconductor switches which limits the switching frequency, output current through the device and, hence, the power output [4]. To overcome the loss balancing problem, a modified version of NPC, known as the active NPC (ANPC) is introduced wherein the clamping diodes are replaced with the switches for balancing losses among the switches [5].

FCs are another class of MLCs where in several charged capacitors are used in generating higher number of voltage levels. The capacitor voltages can be maintained at the desired values using the available switching state redundancies. Here again as the number of levels are increased, more capacitors are needed. These electrolytic capacitors are the weakest link in an inverter. They add to the cost and also make the converter less reliable [6]. There is a tradeoff between the cost of clamping diodes in DC-MLI and the FCs for choosing the topologies for an application. At low switching frequencies, NPC becomes the obvious choice because of the larger capacitor size requirement of FCs.

Another breed of power converters are the CHB converters [2]. They have the least component count compared to DC-MLIs and FCs especially due to absence of any clamping diodes or FCs. But CHB-based topologies reported with single dc supply and multiple floating capacitors in each phase are dependent on load power factor and modulation index for the floating capacitor balancing.

In an attempt to increase the number of levels, several new topologies are introduced by modifying the above basic topologies. By combining three-level ANPC and two-level cell, a new topology with higher number of levels is developed [7]. Another paper discusses about adding a common cross-converter stage between three-level ANPC and the FC and thereby generating more levels [8]. An interesting way of generating higher levels is discussed in [9] by feeding the induction machine with open end stator winding specially for drives application. Also many new hybrid topologies for specific applications are discussed in the

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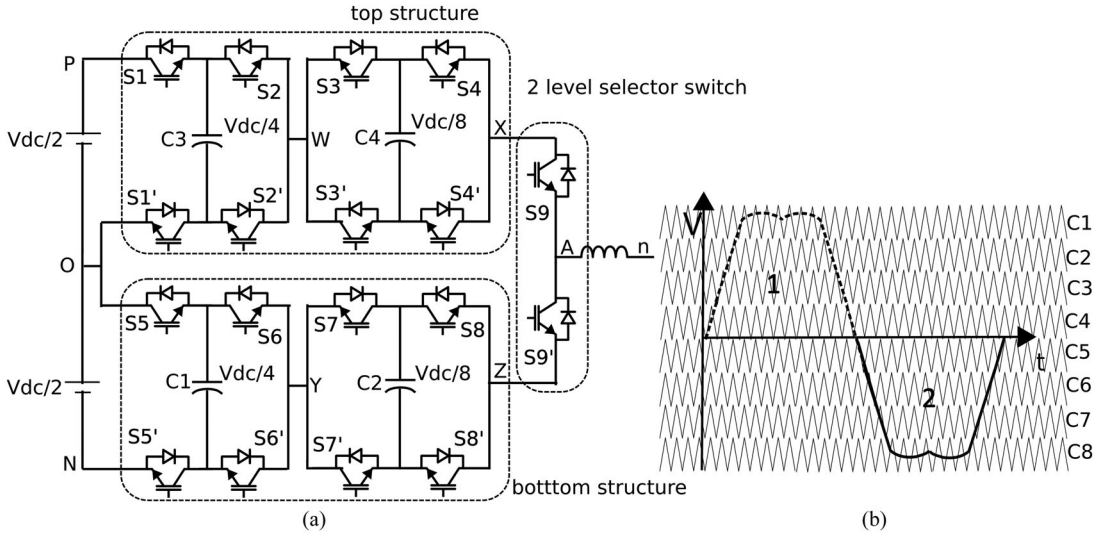

Fig. 1. Power circuit for the proposed stacked nine-level inverter and its modulating signal for phase "a." (a) Proposed 9 level inverter by stacking two 5 level inverters, (b) Signal 1 for modulating the top structure and signal 2 for modulating the bottom structure along with the 8 carriers.

literature [10]–[13]. Stacked multicell converter was introduced to generate more levels. They use less number of capacitors but require more switches [14]. Multilevel structures of 5-level [15], 9-level [13], and 17-level [16] have been reported with a single dc power supply by cascading conventional three-level FC topology and capacitor-fed H bridges with inherent capacitor balancing during inverter switching cycles.

In this paper, a new method of generating higher number of voltage levels by stacking MLCs of lower space vector structures and having a single dc power supply as mentioned earlier with low voltage devices is presented in detail for drives application. The concept can also be generalized for obtaining higher voltage levels. To verify the concept experimentally, a nine-level inverter is developed by stacking two hybrid five-level inverters. The operation, notable features, and experimental results are discussed in the following sections.

II. Inverter Topology and Its Operation

The proposed inverter structure for a nine-level is shown in Fig. 1(a). It is realized by stacking two five-level inverters in each phase. Each of the five-level inverters are obtained by cascading a three-level FC inverter and a capacitor fed H bridge [15]. There are two selector switches in each phase to connect the respective outputs to the induction machine. The FC in each structure has to be maintained at Vdc/4 and H-bridge capacitors have to be maintained at Vdc/8, where Vdc is the dc link for a conventional two-level inverter. The structure overall has nine pairs of complimentary switches in each phase (S1-S1′, S2-S2′ ... S9-S9′). Each of the switches in FC needs to block only Vdc/4 and each of the switches in H bridge needs to block only Vdc/8. The top structure generates five pole voltages with respect to "O" such as levels 0, Vdc/8, 2Vdc/8, 3Vdc/8, 4Vdc/8. Bottom structure also generates same five pole voltages with respect to "N." But with respect to "N," top structure generates five pole voltages which are Vdc/2 added with the above ones. So overall stacked structure generates nine pole voltages (V_{AN}) for phase "a" such as levels 0, Vdc/8, 2 Vdc/8, 3 Vdc/8, 4 Vdc/8, 5 Vdc/8, 6 Vdc/8, 7 Vdc/8, Vdc. Level-shifted carrier-based pulse width modulation (PWM) technique can be used for modulation [17], [18] of the proposed structure.

The operation of the stacked structure is as follows. During the positive half cycle of the reference waveform [signal-1 in Fig. 1(b)], the bottom structure is clamped to the midpoint "O" by turning ON S5, S6, S7, S8. Because of this operation, the voltage rating of S9′ has to be Vdc/2 only. The selector switches S9 is kept ON and S9′ is OFF during this period. Now the top structure will switch to generate the required pole voltages. Similarly during the negative half cycle [signal-2 in Fig. 1(b)], the top inverter structure is clamped to the midpoint "O" by turning ON S1′, S2′, S3′, S4′. S9′ is kept ON and S9 is permanently kept OFF. Again S9 has to be rated for only Vdc/2. Here, the bottom structure will switch to generate the required pole voltages. So the selector switches are switching at line frequency only. The selector switches switch only during the zero crossing of the modulating signal. When the modulating signal is transiting from positive half cycle to negative half cycle, the upper selector switch has to go OFF and bottom selector switch has to turn ON. During this transition, it can be seen that all the top switches of the bottom structure (S5, S6, S7, S8) and all the bottom switches of the top structure (S1′, S2′ S3′, S4′) are ON. If S9′ is turned ON just before S9 turns OFF, S9 can undergo a zero voltage switching OFF. At the same time, S9′ is undergoing a zero voltage switching ON as shown in Fig. 2. The darkened switches in the figure are ON. The figures from (a) to (c) represent this transition shown using the solid arrow. The reverse transition from negative half cycle to positive half cycle can also be made zero voltage switching by going through the intermediate state (b), shown using the dotted arrow. Hence, the selector switches do not add to any switching loss.

The proposed structure for nine-level shown in Fig. 1(a) requires 54 switches although the six selector switches are switching at line frequency without causing any switching loss and all the remaining switches are operating only in one half cycle.

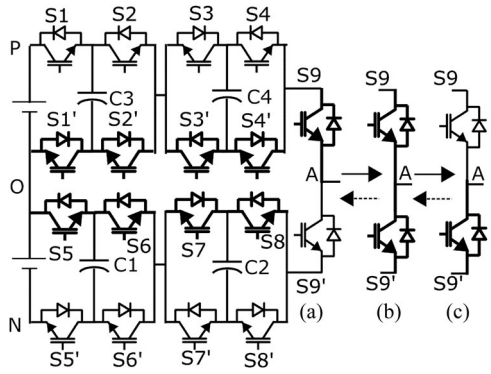

Fig. 2. Transition states during zero crossing of modulating signal to eliminate switching loss in the selector switches. The solid arrow shows transition from positive to negative half cycle. The dotted arrow shows transition from negative to positive half cycle. All the darkened switches are ON.

TABLE I
SWITCHING STATE REDUNDANCIES FOR THE POLE VOLTAGES AND THEIR EFFECT ON THE CAPACITOR VOLTAGES

S.No	Switch States	V_{AN}	I_a	C1	C2
1	0000 0000 0	0	+	U	U
2	0000 0011 0	0	+	U	U
3	0000 0001 0	Vdc/8	+	U	D
4	0000 0110 0	Vdc/8	+	D	C
5	0000 1010 0	Vdc/8	+	C	C
6	0000 0100 0	Vdc/4	+	D	U
7	0000 0111 0	Vdc/4	+	D	U
8	0000 1000 0	Vdc/4	+	C	U
9	0000 1011 0	Vdc/4	+	C	U
10	0000 0101 0	3Vdc/8	+	D	D
11	0000 1001 0	3Vdc/8	+	C	D
12	0000 1110 0	3Vdc/8	+	U	C
13	0000 1100 0	Vdc/2	+	U	U
14	0000 1111 0	Vdc/2	+	U	U
15	0000 1111 1	Vdc/2	+	U	U
16	0011 1111 1	Vdc/2	+	U	U
17	0001 1111 1	5Vdc/8	+	U	D
18	0110 1111 1	5Vdc/8	+	D	C
19	1010 1111 1	5Vdc/8	+	C	C
20	0100 1111 1	3Vdc/4	+	D	U
21	0111 1111 1	3Vdc/4	+	D	U
22	1000 1111 1	3Vdc/4	+	C	U
23	1011 1111 1	3Vdc/4	+	C	U
24	0101 1111 1	7Vdc/8	+	D	D
25	1001 1111 1	7Vdc/8	+	C	D
26	1110 1111 1	7Vdc/8	+	U	C
27	1100 1111 1	Vdc	+	U	U
28	1111 1111 1	Vdc	+	U	U

Note: "U" - Unaffected, "C"- Charging, "D" - Discharging. "+" indicates current flow from inverter pole "A" to machine neutral "n." Switch State is defined as (S1 S2 S3 S4 S5 S6 S7 S8 S9). "1" indicates switch is ON and "0" indicates switch is OFF.

Also this inverter has a modular structure, since the H bridges can be bypassed if it fails and the inverter can still operate in the entire modulation range with lower number of voltage levels.

III. CAPACITOR VOLTAGE BALANCING

The capacitor voltages need to be maintained at the respective levels for generating the pole voltages [19]. Each of the

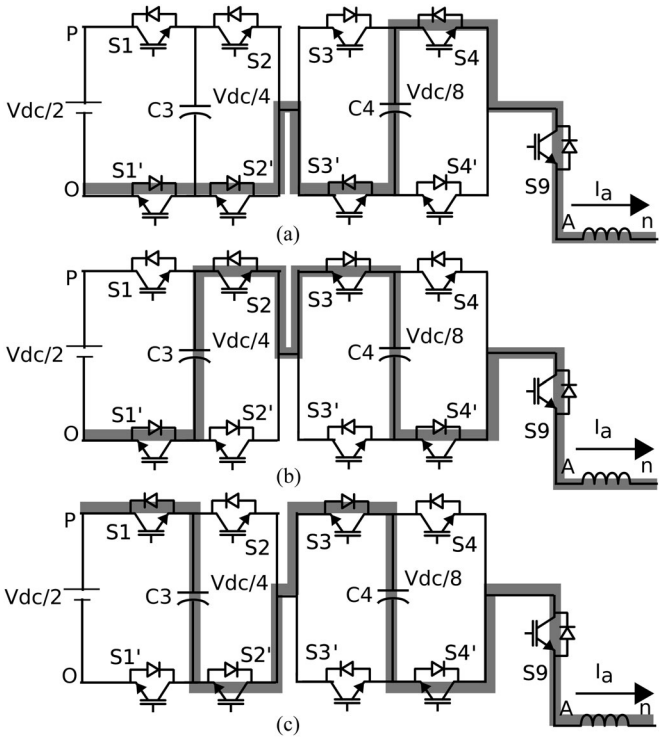

Fig. 3. Switching redundancies available for a pole voltage. (a), (b), and (c) show current paths and charge and discharge of capacitors for switching redundancies available for pole voltage of 5Vdc/8.

capacitor voltages in the topology has to be maintained at their reference values. Hence, we define a small hysteresis band [15] for each of the capacitor voltage references and maintains the voltages within this band using the available switching state redundancies. During a sampling instant, if the capacitor charges and reaches the upper limit of the hysteresis band, immediately in the next sampling instant, the switching state is changed to discharge that capacitor. Since, the capacitors are designed considering the switching frequency, peak of load current, and the voltage deviation, the capacitor voltages always lie within the hysteresis band.

The steady-state operation of the top and bottom structure in Fig. 1(a) are similar and, hence, the capacitor voltage balancing algorithm is also similar. For the topology, there are switching state redundancies available for generating a pole voltage. These redundancies can either charge or discharge a capacitor while maintaining the same pole voltage. These redundancies are used to maintain the capacitor voltages. Table I lists all the switching redundancies of all the pole voltages and also their effect on the capacitor voltages for a particular direction of current. As the current reverses, the effect on capacitor voltages also reverses. Fig. 3 shows the use of switching state redundancies to charge and discharge a capacitor for a pole voltage (V_{AN}) of 5Vdc/8. For obtaining 5Vdc/8, the top structure only needs to operate. Hence, only top structure is shown in Fig. 3. From the Table I, it can be seen that for the positive direction of current from "A" to "n," the switching state (0001 1111 1)

TABLE II
SWITCHING STATE SELECTION TABLE BASED ON CURRENT DIRECTION AND CAPACITOR VOLTAGE STATUS FOR PHASE "A"

I_a	H_{a1}/H_{a3}	H_{a2}/H_{a4}	Switching state selection for the various pole voltages					
			Vdc/8	Vdc/4	3Vdc/8	5Vdc/8	3Vdc/4	7Vdc/8
+	0	0	0000 1010 0	0000 1011 0	0000 1110 0	1010 1111 1	1011 1111 1	1110 1111 1
+	0	1	0000 0001 0	0000 1011 0	0000 1001 0	0001 1111 1	1011 1111 1	1001 1111 1
+	1	0	0000 0110 0	0000 0111 0	0000 1110 0	0110 1111 1	0111 1111 1	1110 1111 1
+	1	1	0000 0001 0	0000 0111 0	0000 0101 0	0001 1111 1	0111 1111 1	0101 1111 1
-	0	0	0000 0001 0	0000 0111 0	0000 0101 0	0001 1111 1	0111 1111 1	0101 1111 1
-	0	1	0000 0110 0	0000 0111 0	0000 1110 0	0110 1111 1	0111 1111 1	1110 1111 1
-	1	0	0000 0001 0	0000 1011 0	0000 1001 0	0001 1111 1	1011 1111 1	1001 1111 1
-	1	1	0000 1010 0	0000 1011 0	0000 1110 0	1010 1111 1	1011 1111 1	1110 1111 1

Note: "+" indicates current flow from inverter pole "A" to machine neutral "n." Switch State is defined as (S1 S2 S3 S4 S5 S6 S7 S8 S9) where "1" indicates switch is ON and "0" indicates switch is OFF. H_{ax} = "1" implies capacitor needs discharging and H_{ax} = "0" implies capacitor needs charging to maintain the capacitor voltages within the hysteresis band where $x = 1,2,3,4$.

discharges C4 while C3 is unaffected which is shown in Fig. 3(a). To charge C4, the switching state (0110 1111 1) is used but it discharges C3 which is shown in Fig. 3(b). Again to charge C3, the switching state (1010 1111 1) is used but it charges C4 also which is shown in Fig. 3(c). Whenever the capacitor voltages crosses the hysteresis limits, switching states need to change to maintain the capacitor voltages to desired values. For pole voltages of 0, Vdc/2 and Vdc, none of the capacitors are affected due to the current flow. For all other pole voltages, capacitor voltages change with current flow. Again the application of switching state depends on the present state of capacitor voltages and the current directions. Hence, all the 12 capacitor voltages and currents are sensed. All the capacitor voltages are compared with their references and capacitor voltage status whether it has exceeded the upper or lower limit of the hysteresis band is given by H_{ax}, where $x = 1,2,3,4$ respectively, for C1, C2, C3, and C4. H_{ax} = "1" implies capacitor needs discharging and H_{ax} = "0" implies capacitor needs charging to maintain the capacitor voltages within the hysteresis band. Capacitor voltage status, the required pole voltage, and the current direction decide the switching state at any instant. Table II tells which switching state needs to be applied at any instant depending on the above factors. Thus, instantaneous capacitor voltage control using switch-state redundancies are possible within inverter switching cycle. This is also independent of load power factor.

IV. GENERALIZATION

In the proposed nine-level inverter shown in Fig. 1(a), two five-level inverters are stacked and each five-level inverter is generating half of the total inverter pole voltage. Experimental result showing the modulating signals and the generated pole voltages at 45 Hz operation are shown in Fig. 11. Trace 1 and 2 of Fig. 11 show the total inverter pole voltage and the total modulating signal. Trace 4 and 5 of Fig. 11 show the modulating signal and the inverter pole voltage for the positive half cycle [from the top structure of Fig. 1(a)]. Trace 6 and 7 of Fig. 11 show the modulating signal and the inverter pole voltage for the negative half cycle [from the bottom structure of Fig. 1(a)].

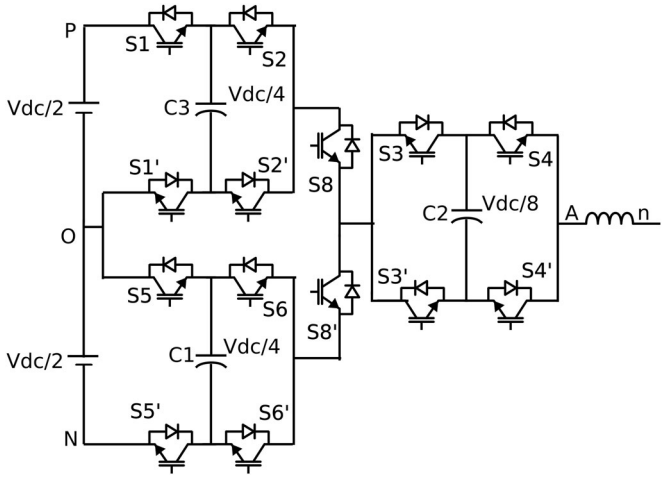

Fig. 4. Modified power circuit to reduce number of switches for the proposed stacked nine-level inverter topology for phase "a."

During the positive half cycle of the reference modulating signal (trace-2 of Fig. 11), the top selector switch is ON and during the negative half cycle, the bottom selector switch is ON, to connect the respective five-level stacked inverter modules to the output. The gate signal to the top selector switch is shown in trace-3 of Fig 11.

To reduce the number of switches, the structure in Fig. 1(a) can be modified as shown in Fig. 4. Here, the H bridge is made common to both the FC and the selector switches are connected in between. Here, the H-bridge switches need to switch throughout the cycle. But they need to block voltage of Vdc/8 only [same as that in Fig. 1(a)]. Therefore, the switching losses are controlled. Also by using redundant H bridges, the system reliability can be improved. This method of stacking can be extended to obtain higher voltage levels. In Fig. 5, a 49-level inverter is shown which is developed by stacking three FC and cascading with three capacitor fed H bridges (which are of lower voltage ratings) through a three-level selector switch. It is shown that an FC cascaded with three H bridges can generate 17 levels [16]. Since there are three stacked 17-level inverters, the reference

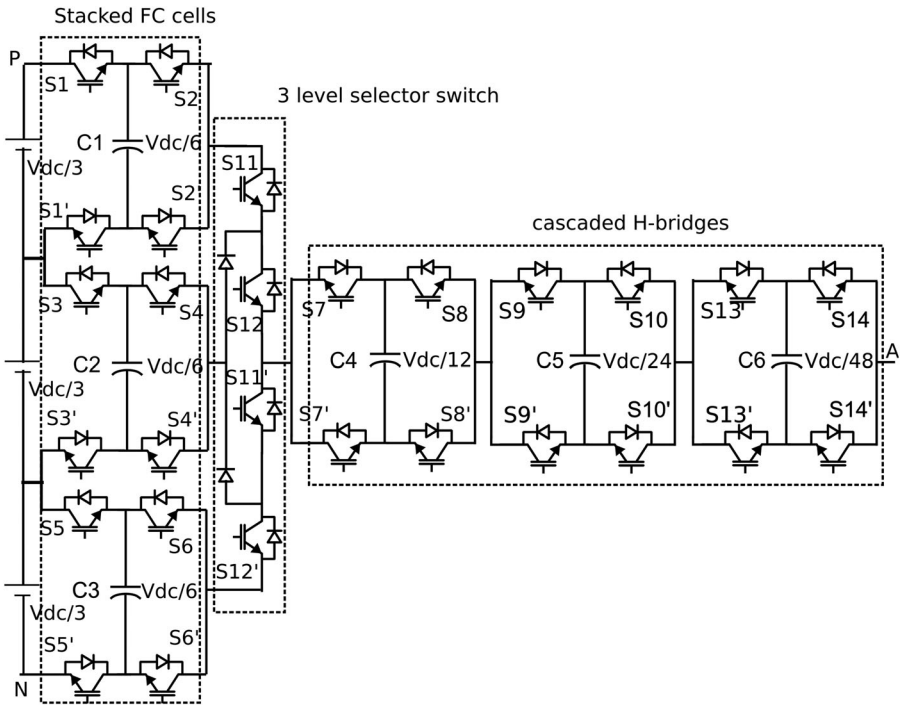

Fig. 5. Power circuit schematic for generation of 49 levels by stacking three FC and cascading with three capacitor fed H bridges of low voltage ratings.

signal has to be divided into three parts and each will be used for modulating each of the 17-level inverter formed by cascading three capacitor fed H bridges with an FC. Hence, this stacked inverter is capable of generating 49 levels (two levels being redundant).

As the number of voltage levels are increased by stacking, the devices need to block only lower voltages and the inverter can be driven directly from battery cells. Also due to the higher number of voltage levels, switching frequency can be reduced and, therefore, higher efficiency is achievable. These advantages will make the stacked inverter structure suitable for application in electric vehicles where the inverter can be driven directly from the stacked low voltage batteries.

V. Comparison With Other Inverter Topologies

The modified nine-level inverter in Fig. 4 is compared with other existing nine-level topologies in this section. The modified proposed topology requires total of 42 switches. Out of which, six selector switches are switching at line frequency and whose switching losses can be minimized using the method discussed in the earlier section. The top and bottom FC is operating only for one half of a fundamental cycle and is idle during the other half.

In the conventional NPC and FC topologies for nine level, many clamping diodes and FCs are required for their operation, respectively. In the proposed structure with less number of floating capacitors, capacitor balancing can be done throughout the modulation range irrespective of any load power factor, whereas in a nine-level NPC, there is a limitation on modulation index due to the capacitor unbalance problem [20], [21]. The basic conventional CHB structure, although requires least number of components among the conventional topologies, needs more number of isolated dc sources. The open end nine-level configuration uses lesser number of switches but it has 12 Vdc/2 switches which have to operate throughout the cycle whereas in the proposed inverter, there are only six Vdc/2 switches (selector switches) and they switch only once in a fundamental cycle and their switching losses are also minimized. In addition, all the Vdc/4 switches in the FC of the proposed inverter operate only in one half of fundamental cycle unlike in the case of an open-end configuration. Again comparing with the standard nine-level ANPC, the switching losses in the Vdc/2 switches (selector switches) in the proposed inverter (6 compared to 12 in ANPC) are highly minimized with zero voltage switching. Also the Vdc/4 switches in the proposed inverter (although 24 in number) operate only in one half of fundamental cycle. The comparison is detailed in Table III.

VI. Experimental Results

A three-phase, 415-V, 7.5-KW, 50-Hz induction motor (IM) is driven with the proposed nine-level inverter shown in Fig. 1(a) using open-loop V/f control scheme. The implementation block diagram is shown in Fig. 6. TMS320F28335 is the processor used for implementing the level-shifted PWM. All the capacitor voltages and currents are sensed using the ADC channels in DSP. The PWM information, level data, capacitor voltage status, and the current directions are encoded and send to Spartan 3 XCS3200 FPGA module which is used for selecting the appropriate switching state from the lookup table stored in the FPGA. Dead time of 2.5 μs is provided between the complimentary signals. All the capacitor voltages are maintained within a ripple of 2%. The capacitance value is given by, $C = I_p T_s / \Delta V_c$ where

TABLE III
COMPARISON OF NINE-LEVEL INVERTER TOPOLOGIES

Topologies	IGBT			Capacitors				Clamping diodes	DC sources		
	Vdc/2	Vdc/4	Vdc/8	Vdc/4	Vdc/8	3Vdc/8	Vdc/2		Vdc	Vdc/2	Vdc/8
Proposed (see Fig. 4)	6	24	12	6	3	0	0	0	0	2	0
NPC	0	0	48	0	8	0	0	168	1	0	0
FC	0	0	48	0	84	0	0	0	1	0	0
Conventional CHB	0	0	48	0	0	0	0	0	0	0	12
Open end 9L [9]	12	12	12	0	9	0	0	0	0	2	0
Standard 9L-ANPC	12	0	24	3	3	3	0	0	0	2	0

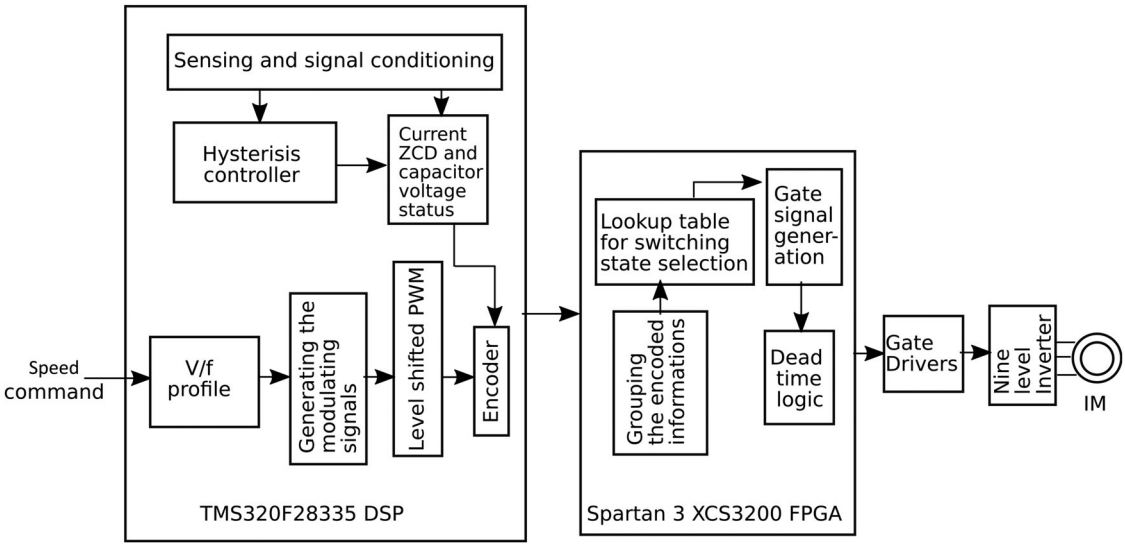

Fig. 6. Block diagram representation of the implemented inverter topology.

C is the capacitance value of C1, C2, C3, C4 in all phases, I_p is the peak load current, ΔV_c is the peak to peak voltage ripple, and T_s is inverter switching time. Capacitance value of 2200 μF is selected for all the capacitors in the experiment. Synchronous PWM technique is implemented for the proposed inverter. Number of samples per cycle is taken as 48 for fundamental frequency ranging from 35 to 45 Hz, 60 for 27 to 35 Hz, 72 for 21 to 27 Hz, and 90 for 17 to 21 Hz, 120 for 13 to 17 Hz, and 180 for 6 to 13 Hz. Samples per cycle should be an integral multiple of 6 so that waveforms will have both half-wave and three-phase symmetry. IM is run at frequencies 10, 20, 30, and 45 Hz with reference voltage tracing different layers in the space vector structure. Experimental results showing the inverter phase voltages (trace-1), pole voltages with respect to midpoint "O" (trace-2), the FC voltage ripple of top structure (trace-3) and phase current (trace-4) for "a" phase are shown for 10-Hz operation [see Fig. 7(a)], 20-Hz operation [see Fig. 7(b)], 30-Hz operation [see Fig. 7(c)], and 45-Hz operation [see Fig. 7(d)]. It can be seen in the above figures that as the speed command is increased from 10 to 45 Hz, the number of levels in the pole voltage waveform (trace-2) increases from 3 to 9. All the experimental results shown are at no load since no load operation gives worst case current ripple. Capacitor voltage ripple for three of the capacitors (traces 1-3) during 10 and 45 Hz operation are shown separately in Fig. 8. Transient results showing the acceleration of motor from 10 to 45 Hz in 2.5 s and the capacitor voltages during this transient are shown in Fig. 9(a). During the acceleration, the phase voltage waveform (trace-1) shows a linear rise and the phase current (trace-4) remains constant. The capacitor voltages (traces 2, 3) are controlled within the band during the operation. To test the capacitor voltage balancing algorithm, the balancing algorithm is intentionally disabled at Td and then enabled at Te as shown in Fig. 9(b). It can be noticed that capacitor voltages (traces 2, 3) return to their reference values in less than 1 s at Tss. Capacitor balancing algorithm takes care of the capacitor voltage build up during starting. Hence, no precharging circuitry is needed. Experimental result showing the capacitor voltage build up during starting is shown in Fig. 10(a). The voltages of the capacitors in FC and H bridge of top structure (traces 2,3) are building up to their desired values in less than 4 s. In Fig. 10(b), the reduced switching of FC and the H bridge to maintain the respective capacitor voltages to desired values at 45-Hz operation is shown. Trace-1 shows the total modulating signal. Traces-2 and 3 show the top and bottom FC pole voltages with respect to midpoint "O." Traces-4 and 5 show the top and bottom H-bridge switchings. It can also be observed from Fig. 10(b) that the two stacked cells are switching only for one half of the fundamental cycle.

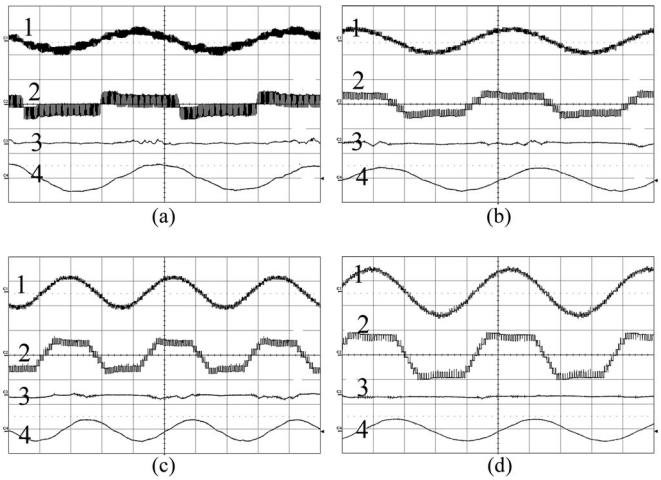

Fig. 7. Motor Phase voltage (V_{An}), Inverter pole voltage (V_{AO}), Capacitor voltage ripple (ΔV_{c3}), Phase current (I_a) for phase A for different modulation indices. (b), (c) and (d) *y*-axis 1) V_{An}: 100 V/div, 2) V_{AO}: 100 V/div 3) ΔV_{c3}: 5 V/div 4) I_a: 2 A/div. (a) *y*-axis 1) V_{An}: 50 V/div, 2) V_{AO}: 50 V/div 3) ΔV_{c3}: 5 V/div 4) I_a: 2 A/div. (a) 10 Hz operation, x–axis: 20 ms/div, (b) 20 Hz operation, x–axis: 10 ms/div, (c) 30 Hz operation, x–axis: 10 ms/div, (d) 45 Hz operation, x–axis: 5 ms/div.

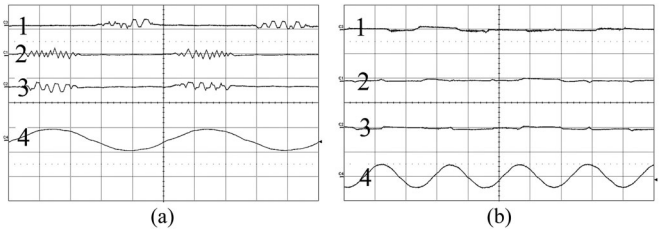

Fig. 8. Capacitor voltages ripple and motor phase current for "a" phase. *y*-axis: 1) ΔV_{c1}: 5 V/div, 2) ΔV_{c3}: 5 V/div, 3) ΔV_{c4}: 5 V/div, 4) I_a: 2 A/div. (a) 10 Hz, *x*-axis: 20 ms/div. (b) 45 Hz, *x*-axis: 10 ms/div.

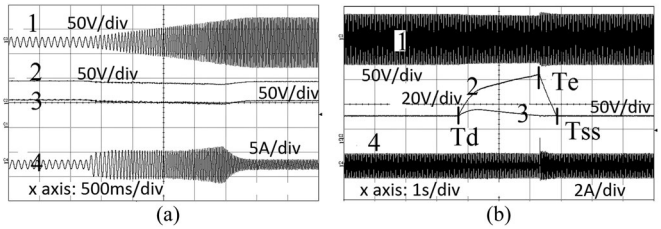

Fig. 9. (a) Motor acceleration. (b) Intentional capacitor unbalancing. *y*-axes: 1) Motor Phase voltage (V_{An}), 2) Capacitor voltage V_{c4}, 3) Capacitor voltage V_{c3}, 4) Phase current (I_a).

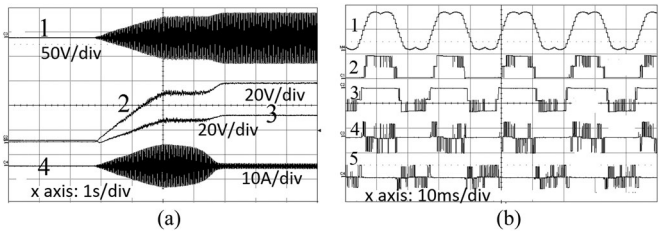

Fig. 10. (a) Motor starting transients. *y*-axis: 1) Motor Phase voltage (V_{An}), 2) Capacitor voltage V_{c3}, 3) Capacitor voltage V_{c4}, 4) Phase current (I_a). (b) Individual FC pole voltages (traces-2,3) and Individual H-bridge switchings (traces-4,5). 1) Modulating signal, 2) V_{WO}, 100V/div, 3) V_{YO}, 100V/div, 4) V_{XW}, 20V/div, 5) V_{ZY}, 50V/div.

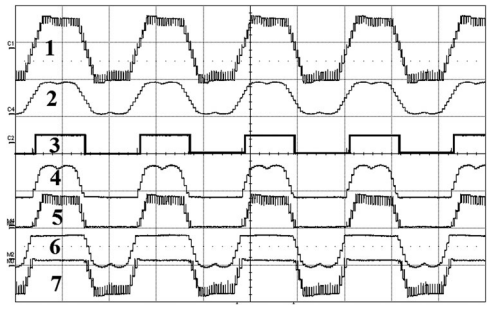

Fig. 11. Modulating signals and the generated pole voltages by each of the stacked cells and the inverter at 45 Hz operation. *x*-axis: 10 ms/div. 2) V_{AO}, 100 V/div, 3) Gating signal, 50 V/div, 5) V_{XO}, 100 V/div, 7) V_{ZO}, 100 V/div.

VII. Conclusion

In this paper, a new method of generating higher number of voltage levels by stacking MLCs having lower space vector structures is presented. Here, each of the stacked inverter is having only one dc supply. The proposed stacked MLI has a modular structure which is realized by stacking the FC and cascading it with series-connected capacitor fed H bridges. Since the voltage across the H-bridge switches are low, the switching loss can be further reduced. Also the H bridges can be bypassed if it fails. Thus, using this system has an improved reliable operation. Also when one of the FC fails, inverter can still be operated with reduced voltage and power levels. The concept of stacking can be generalized to obtain higher voltage levels. As the number of levels increases, blocking voltages of switches reduces and the proposed structure can be fed from low voltage battery cells. Also, higher number of voltage levels imply lower switching frequency and, therefore, higher efficiency, which makes it suitable for application in electric vehicles. Hysteresis based capacitor voltage balancing algorithm is used to maintain the capacitor voltages irrespective of modulation index and load power factor. Detailed experimental results, using a stacked nine-level inverter, showing the steady-state operation at different frequencies and the transient results, ensure that the proposed structure will be a viable scheme for high power applications with improved reliability.

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